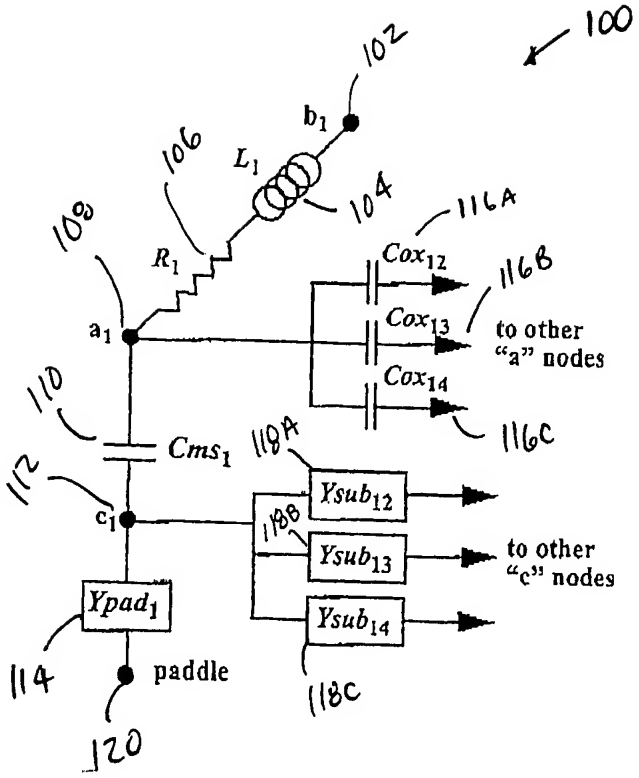

100
102
b_1
L_1
106
104
108
R_1
116A
Cox_{12}
116B
Cox_{13}
to other "a" nodes
Cox_{14}
116C
a_1
110
Cms_1
118A
$Ysub_{12}$
112
c_1
118B
$Ysub_{13}$
to other "c" nodes
$Ypad_1$
$Ysub_{14}$
114
paddle
118C
120

FIG. 1

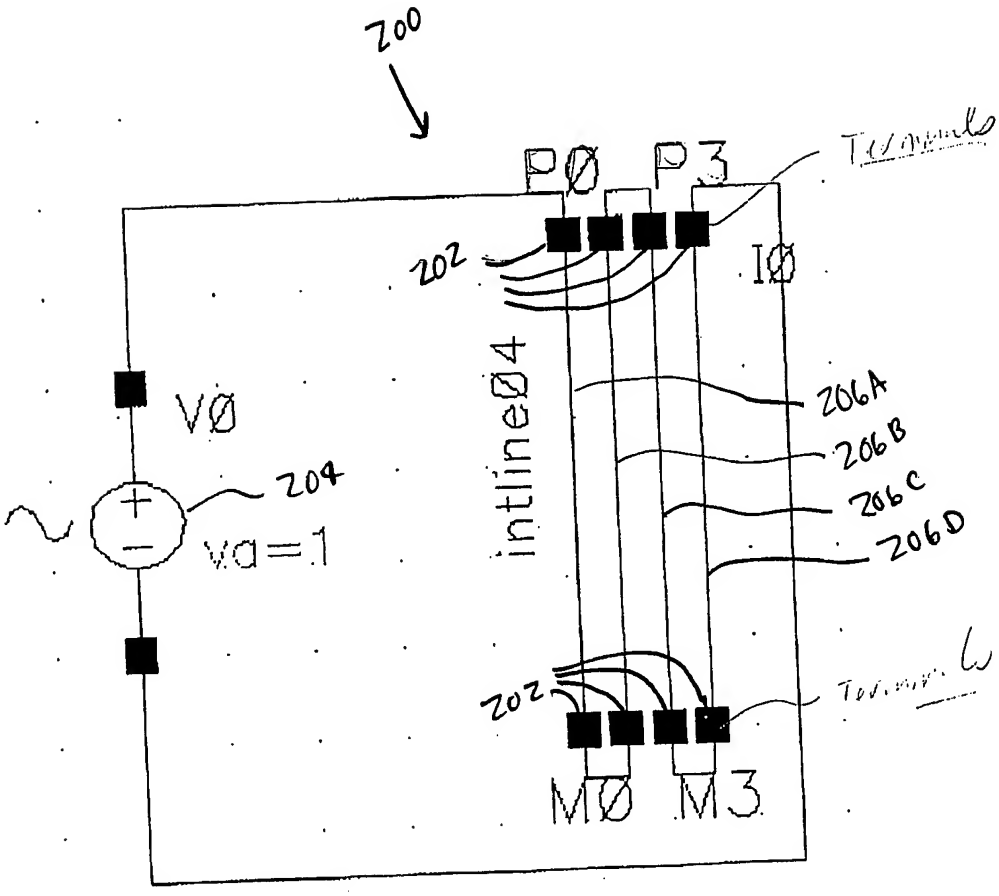

200
P0
P3
Terminals
202
I0
intline04
206A
206B
206C
206D
V0
204
va=1
202
Terminals
M0
M3

FIG. 2

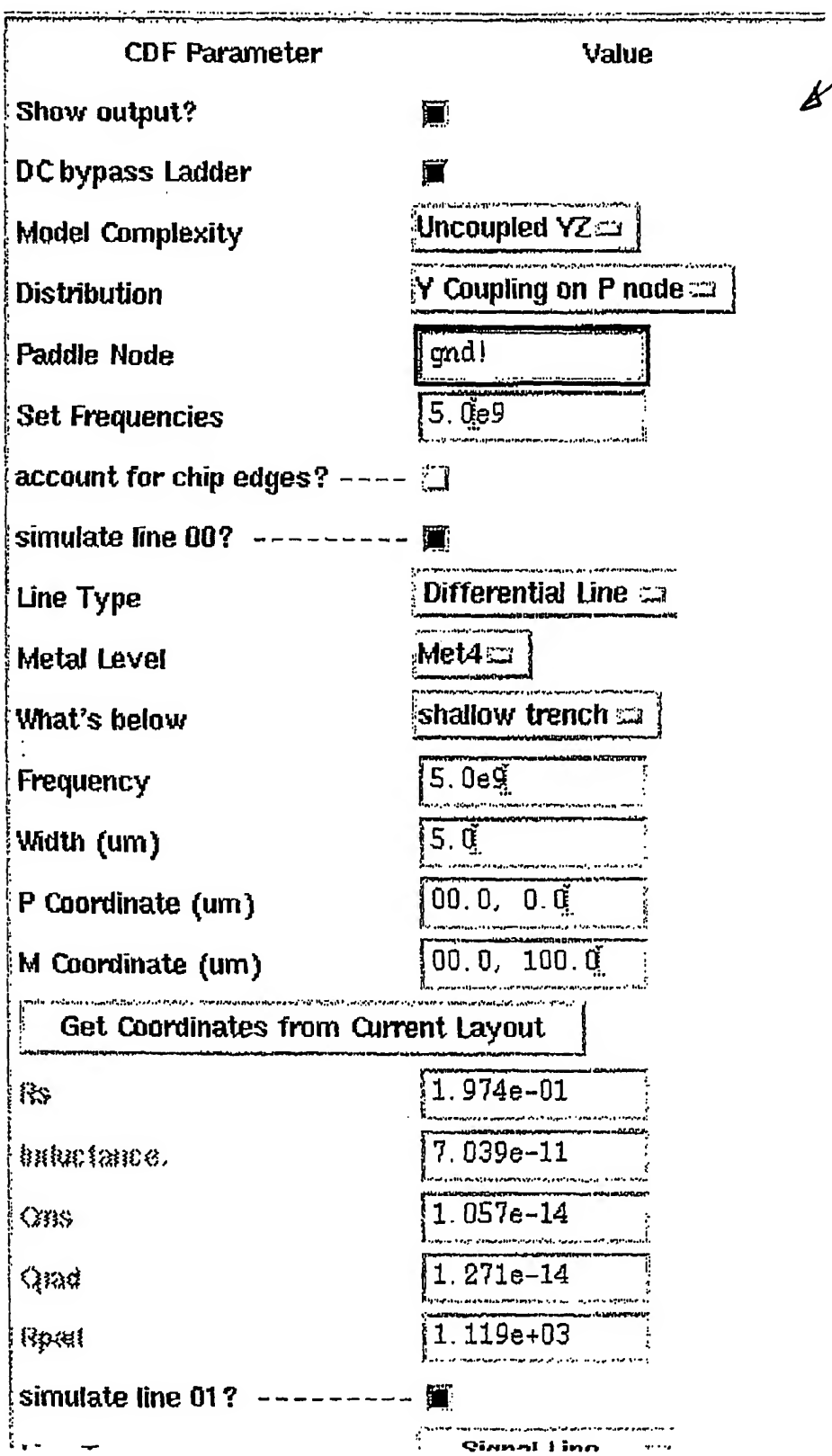
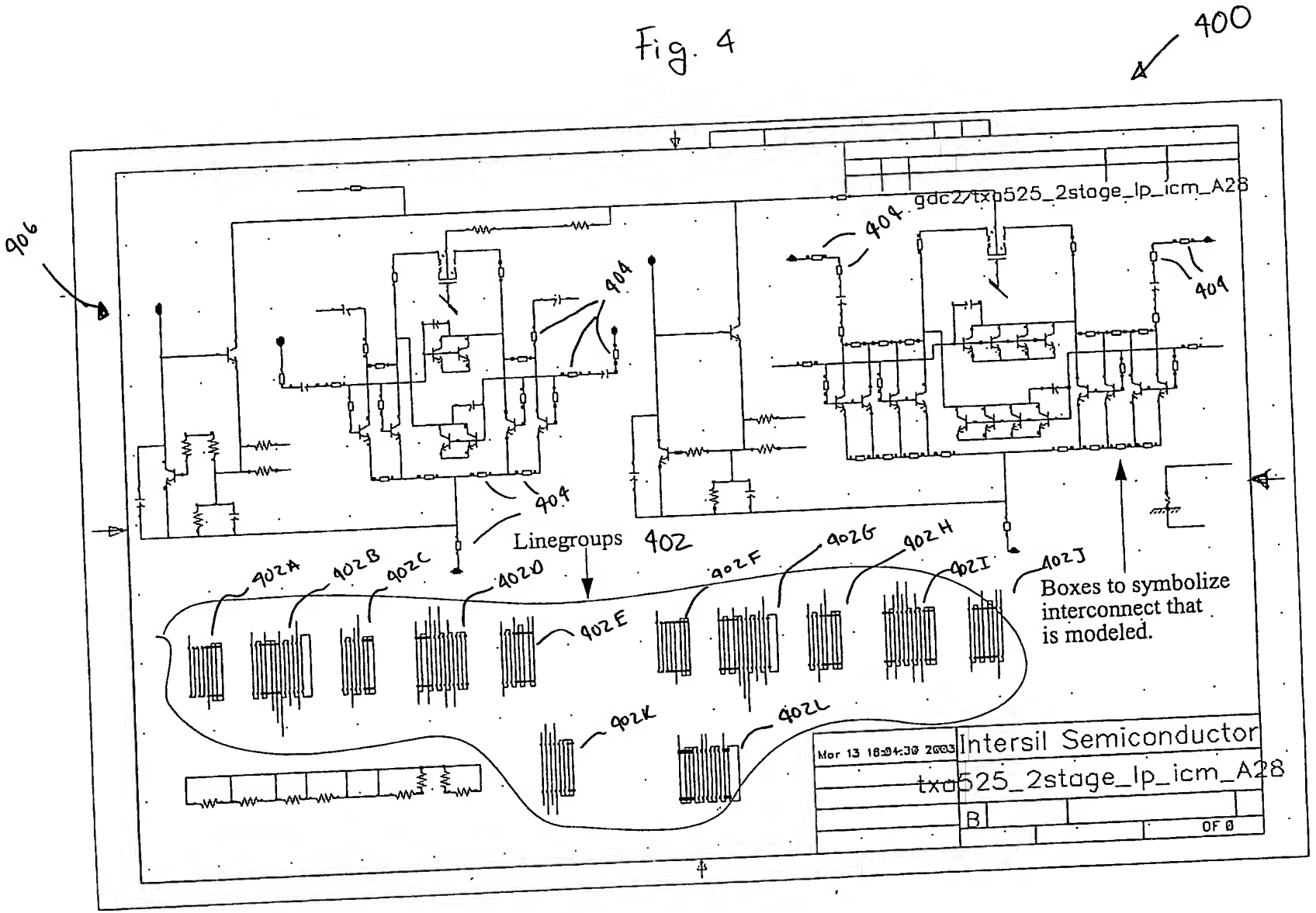

300
CDF Parameter
Value
Show output?
DC bypass Ladder
Model Complexity
Uncoupled YZ
Distribution
Y Coupling on P node
Paddle Node
gnd!
Set Frequencies
5.0e9
account for chip edges? ----
simulate line 00? ---------
Line Type
Differential Line
Metal Level
Met4
What's below
shallow trench
Frequency
5.0e9
Width (um)
5.0
P Coordinate (um)
00.0, 0.0
M Coordinate (um)
00.0, 100.0
Get Coordinates from Current Layout
Rs
1.974e-01
Inductance
7.039e-11
Cms
1.057e-14
Cpad
1.271e-14
Rpcl
1.119e+03
simulate line 01? ---------

Fig 3

Fig. 4


400
906
gdc2/txo525_2stage_lp_icm_A28
404
409
Linegroups 402
402A
402B
402C
402D
402E
402F
402G
402H
402I
402J
402K
402L
Boxes to symbolize interconnect that is modeled.
Mar 13 18:04:30 2003
Intersil Semiconductor
txo525_2stage_lp_icm_A28
B
OF 0

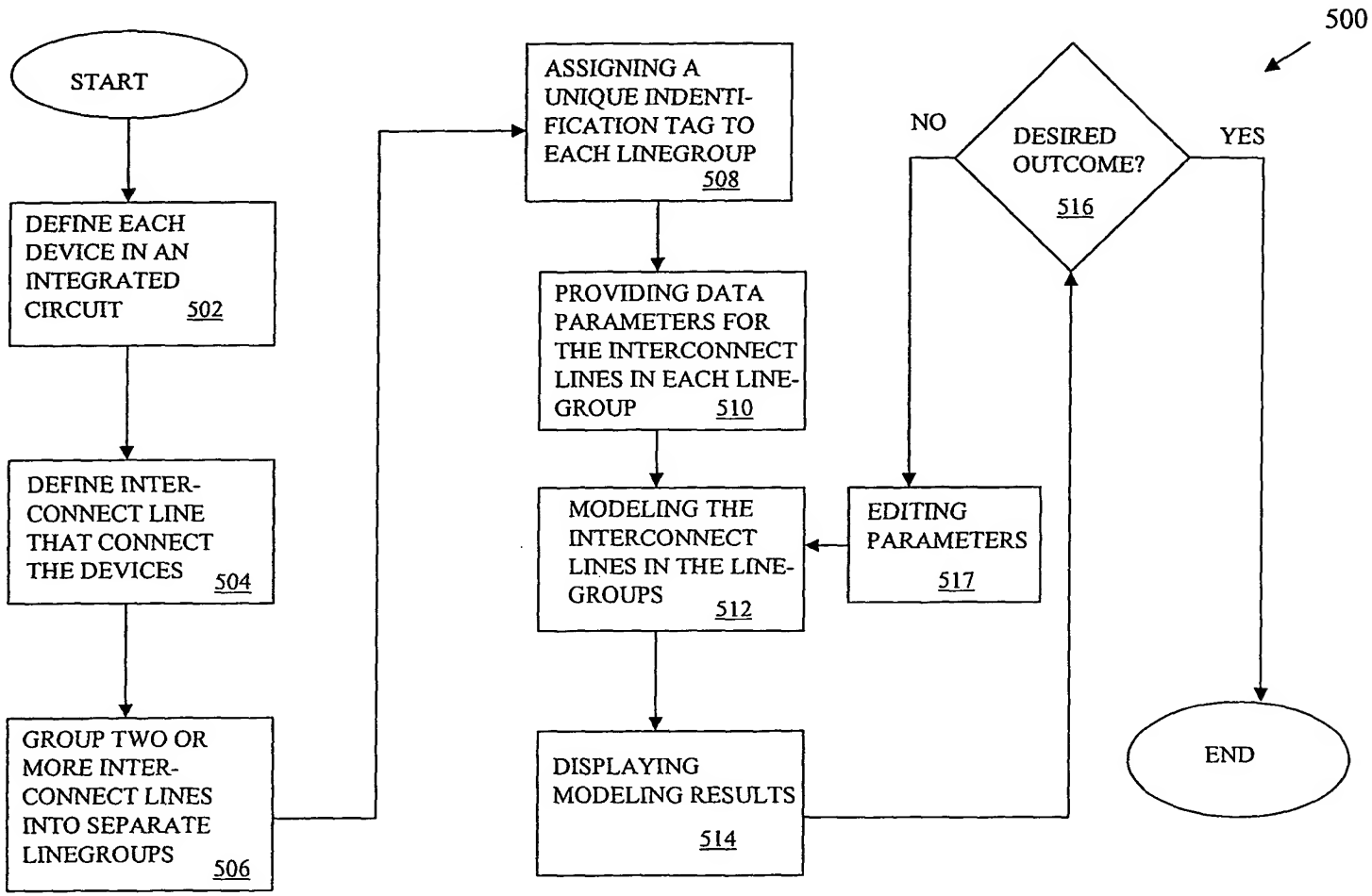

500
START
DEFINE EACH DEVICE IN AN INTEGRATED CIRCUIT 502
DEFINE INTER-CONNECT LINE THAT CONNECT THE DEVICES 504
GROUP TWO OR MORE INTER-CONNECT LINES INTO SEPARATE LINEGROUPS 506
ASSIGNING A UNIQUE INDENTI-FICATION TAG TO EACH LINEGROUP 508
PROVIDING DATA PARAMETERS FOR THE INTERCONNECT LINES IN EACH LINE-GROUP 510
MODELING THE INTERCONNECT LINES IN THE LINE-GROUPS 512
DISPLAYING MODELING RESULTS 514
DESIRED OUTCOME? 516
NO
YES
EDITING PARAMETERS 517
END

FIG. 5